

2001年 9月27日 20時34分

KOSHIBA & PARTS

NO. 6127 P. 2

#10/Translation  
10/10/01  
V. Vannell



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Akitaka KIMURA

Serial No.: 09/161,981

Filed: 29th September, 1998

Group Art Unit: 2812

Examiner: S. Mulpuri

For: SEMICONDUCTOR LAYER  
FORMED BY SELECTIVE  
DEPOSITION AND  
METHOD FOR DEPOSITING  
SEMICONDUCTOR LAYER

TRANSLATOR'S DECLARATION


Honorable Commissioner of Patents  
and Trademarks  
Washington, D. C. 20231

Sir:

I, Toyoaki SATOH, of 2F, Hirakawa-cho KS Bldg., 2-4-14, Hirakawa-cho, Chiyoda-ku, Tokyo 102-0093 JAPAN, hereby certify that I am conversant with both the Japanese and the English languages, and I have prepared the attached English translation of Japanese Patent Application No. Heisei 9-264225 filed on 29th September 1997, and that the English translation is a true, faithful and exact translation of the corresponding Japanese language document.

I further declare that all statements made in this declaration of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of this application or any Patent issued thereon.

September 27, 2001  
Date

  
Name: Toyoaki SATOH

**Patent Office**

**Japanese Government**

**This is to certify that the annexed is a true copy of the following application as filed with this office.**

**Date of Application:** 29th September 1997  
**Application Number:** Patent Application  
No. 264225 of Heisei 9 (1997)  
**Applicant:** NEC Corporation

**10th April 1998**

**Commissioner,  
Patent Office**

**Hisamitsu ARAI**